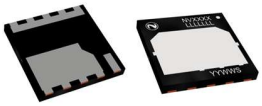
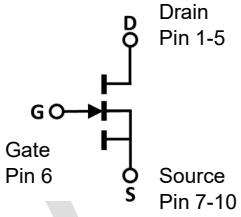
GaNFast™ Power FET

CERTIFIED CARBON NEUTRAL company CarbonNeutral.com

Top-cooled
DFN 8x8 mm





Simplified Diagram

1. Features

- eMode GaN power FET
  - V_{DS} 650V continuous / 800V transient
  - 17 mΩ $R_{DS(ON)_TYP_25C}$
  - 8x8 mm thermally-enhanced, top-cooled
  - Zero reverse-recovery charge
  - Up to 2 MHz operation
  - V_{DS} dV/dt immunity up to 200 V/ns
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

- Residential Solar Micro Inverters and ESS
- AC-DC, DC-DC, DC-AC topologies
- CCM BTP PFC and LLC topologies

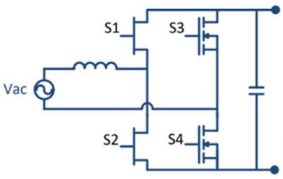
3. Description

NV6034 is a high performance eMode GaNFET that achieves excellent high-frequency and high efficiency operation.

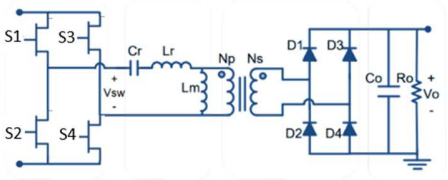
NV6034 also implements a thermally-enhanced top-cooled SMD.

NV6034 is the ideal choice for topologies utilizing MHz+ F_{SW} for high efficiency LLC and other ZVS topologies, to achieve unprecedented power density and cost-effective system BOM, in Consumer, Enterprise, and Solar segments.

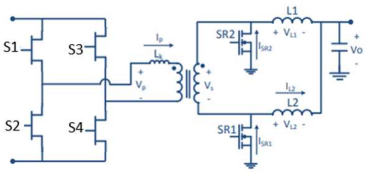
4. Typical Application Circuits



BTP PFC



CLLC or LLC



PSFB or DAB

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5. Table of Contents

(1) Features pg. 1
(2) Applications / Topologies pg. 1
(3) Description pg. 1
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6. Absolute Maximum Ratings (Note 1) (with respect to Source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{DS_(CONT)}$	Continuous Drain-to-Source voltage	-7 to +650	V
$V_{DS_(TRAN)}$	Transient Drain-to-Source voltage (Note 2)	800	V
V_{GS}	Continuous Gate-to-Source Voltage	-10 to +7.0	V
$V_{GS_(TRAN)}$	Transient Gate-to-Source Voltage	-20 to +10	V
$I_{DS_(CONT)}$	Continuous current (T_{CASE} = 25 °C) Continuous current (T_{CASE} = 100 °C)	130 80	A
$I_{DS_(PULSE)}$	Pulsed current (10 µs @ T_{JUNC} = 25 °C) Pulsed current (10 µs @ T_{JUNC} = 150 °C)	175 80	A
dV/dt	Drain-to-Source Slew Rate	200	V/ns
T_{JUNC}	Operating Junction Temperature	-40 to +150	°C
T_{STOR}	Storage temperature	-55 to +150	°C

(1) Absolute Maximum Ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS_(TRAN)}$ allows for surge ratings during non-repetitive events that are < 100 µs. Refer to Application Section for recommended design guidelines.

7. Thermal Resistance

Symbol	Parameter	Typ	Units
$R_{e_JUNC-CASE}$	Junction-to-Case Thermal Resistance, Top	0.13	°C/W
	Junction-to-Case Thermal Resistance, Bottom	2.22	

preliminary

8. Electrical Characteristics

Conditions unless specified: V_{DS} = 400V, V_{GS} = 6.0V, T_{CASE} = 25°C, I_{DS} = 29A

Symbol	Parameter	Min	Typ	Max	Units	Conditions
GaN Switch Characteristics						
I_{DSS}	Drain-Source leakage current		1.5	100	µA	V_{DS} = 650 V, V_{GS} = 0 V
I_{DSS}	Drain-Source leakage current		32		µA	V_{DS} = 650 V, V_{GS} = 0V, T_{JUNC} = 150 °C
I_{GSS}	Gate-Source leakage current		150		µA	V_{GS} = 6.0V
$R_{DS(ON)}$	Drain-Source resistance		17	25	mΩ	V_{GS} = 6.0V, I_{DS} = 29A
$V_{GS(th)}$	Gate Threshold voltage		1.5	2.8	V	I_{DS} = 35mA, V_{DS} = 0.1V
V_{SD}	Source-Drain Reverse voltage		3.3	5	V	V_{GS} = 0V, I_{SD}=29A
Q_{RR}	Reverse recovery charge		Zero		nC	
R_G	Internal Gate Resistance		0.1		Ω	
C_{ISS}	Input capacitance		560		pF	V_{DS} = 400 V, V_{GS} = 0V
C_{OSS}	Output capacitance		136		pF	V_{DS} = 400V, V_{GS} = 0V
C_{RSS}	Reverse Transfer capacitance		1.2		pF	V_{DS} = 400V, V_{GS} = 0V
Q_{GATE}	Total Gate charge		14.9		nC	V_{DS} = 400V, V_{GS} = 0V to 6.0V
Q_{GS}	Gate-to-Source charge		2.6		nC	V_{DS} = 400V, V_{GS} = 0V to 6.0V
Q_{GD}	Gate-to-Drain charge		4.3		nC	V_{DS} = 400V, V_{GS} = 6.0V
Q_{OSS}	Output charge		118		nC	V_{DS} = 400V, V_{GS} = 0V
$C_{O(er)}$ (Note 4)	Effective output capacitance, energy related		190		pF	V_{DS} = 400V, V_{GS} = 0V
$C_{O(tr)}$ (Note 5)	Effective output capacitance, time related		295		pF	V_{DS} = 400V, V_{GS} = 0V

(4) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(5) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

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9. Electrical Curves (GaN FET, T_{CASE} = 25 °C unless otherwise specified)

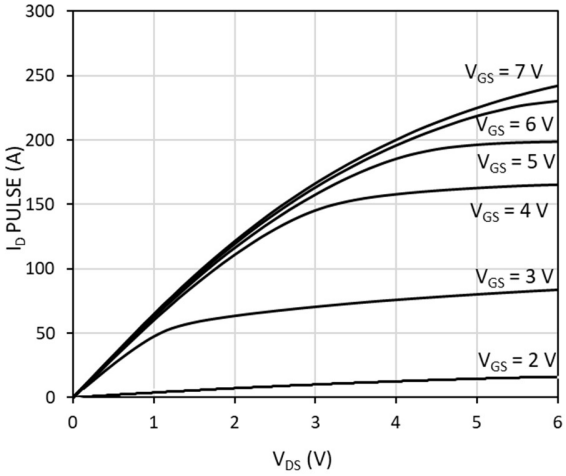


Fig. 1. I_{DS_PULSE} vs. V_{DS} , T_{JUNC} = 25 °C

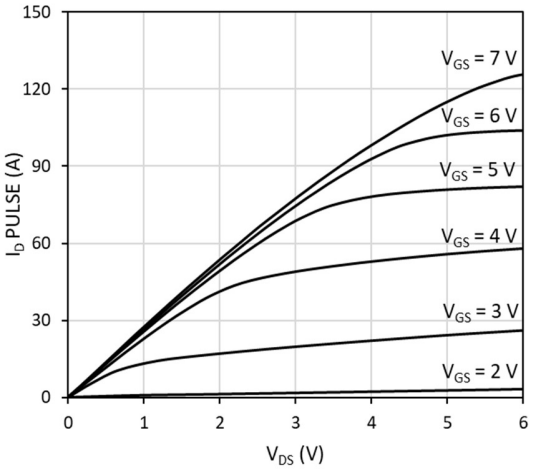


Fig. 2. I_{DS_PULSE} vs. V_{DS} , T_{JUNC} = 150 °C

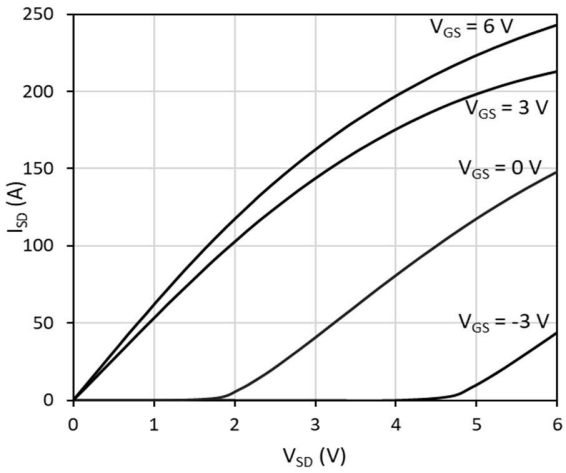


Fig. 3. V_{SD} (reverse conduction), T_{JUNC} = 25 °C

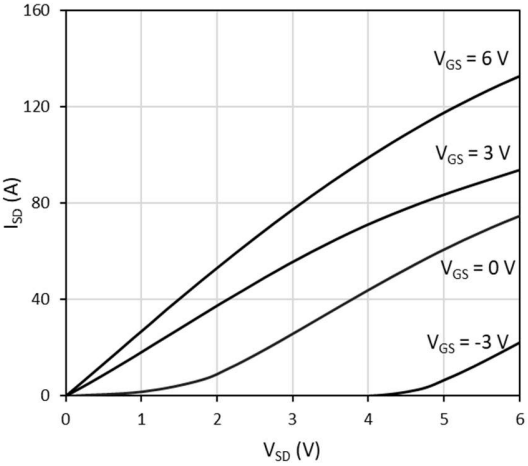


Fig. 4. V_{SD}, T_{JUNC} = 150 °C

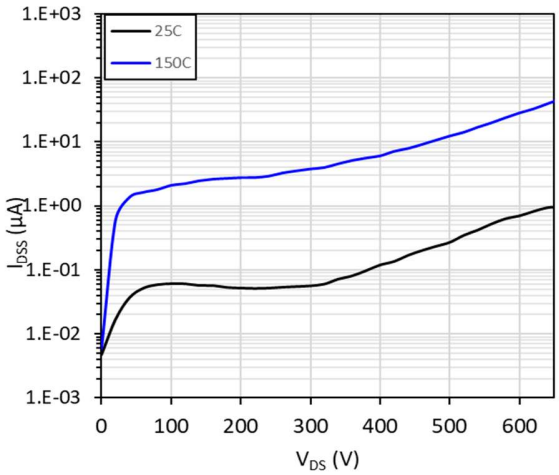


Fig. 5. I_{DSS} vs. V_{DS} (V_{GS} = 0V), T_{JUNC} = 25 °C, 150 °C

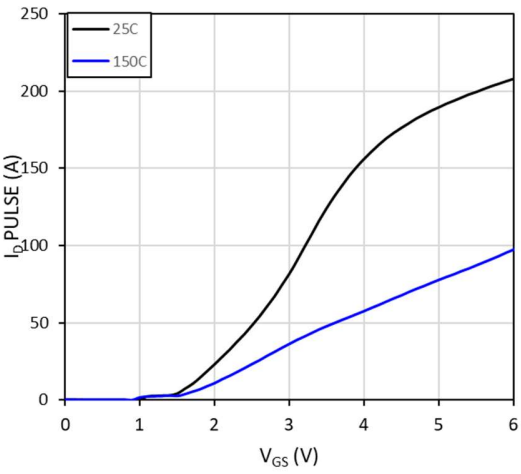


Fig. 6. I_{DS_PULSE} vs. V_{GS}

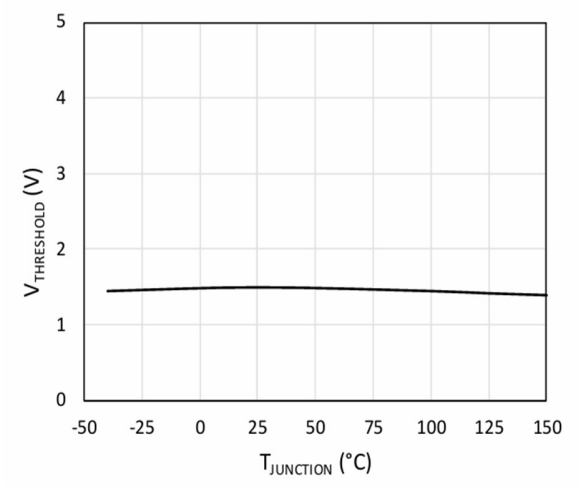


Fig. 7. $V_{GS(th)}$ vs. T_{JUNC}

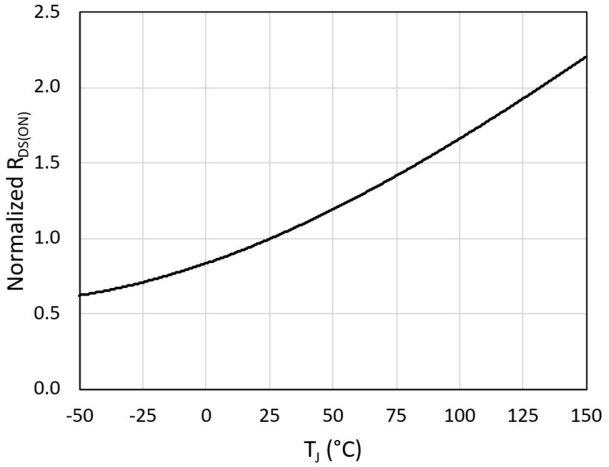


Fig. 8. Normalized $R_{DS(ON)}$ vs. T_{JUNC}

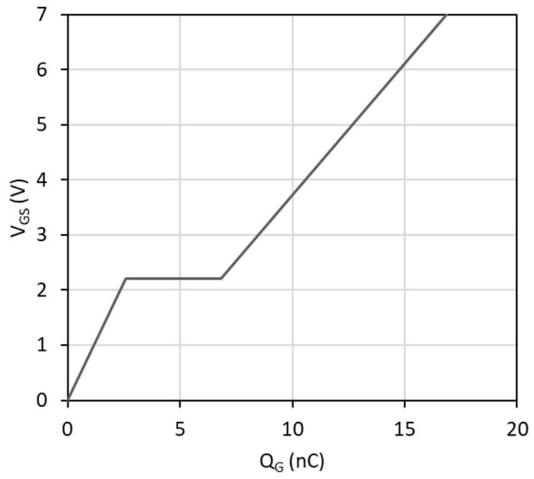


Fig. 9. V_{GS} vs. Q_{GATE}

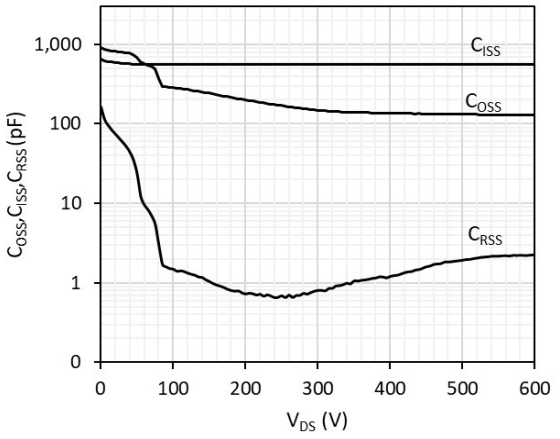


Fig. 10. C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

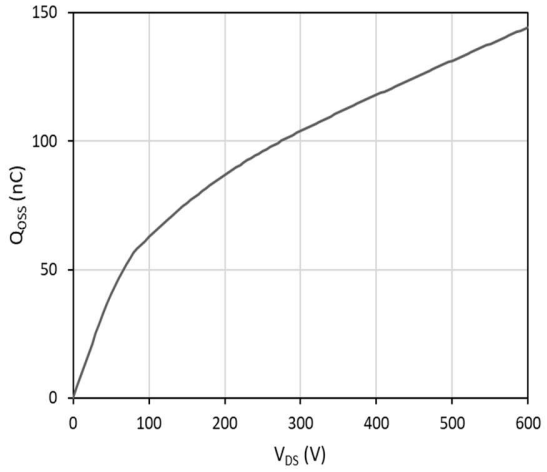


Fig. 11. Q_{OSS} vs. V_{DS}

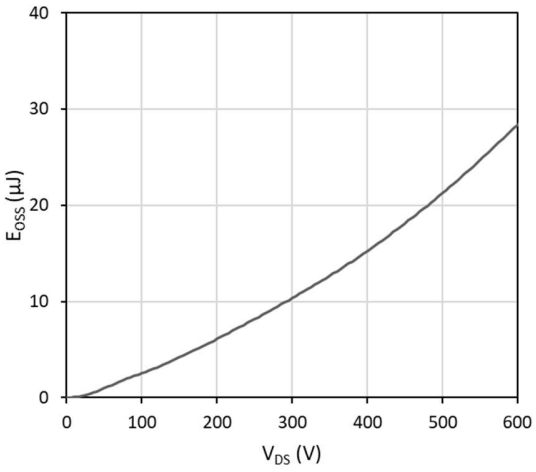


Fig. 12. E_{OSS} vs. V_{DS}

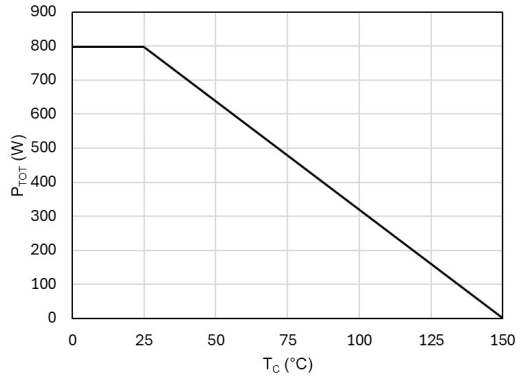


Fig 13. $P_{DISSIPATION}$ vs. T_{CASE}

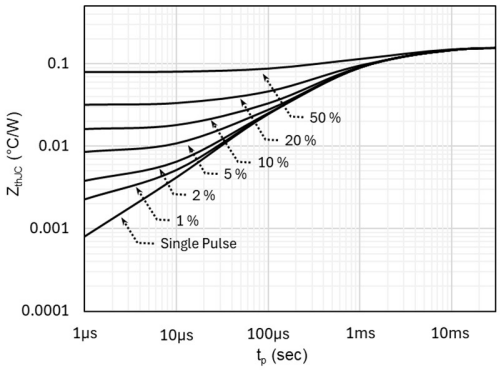


Fig. 14. Transient $R_{\Theta_JUNC\text{-}CASE}$

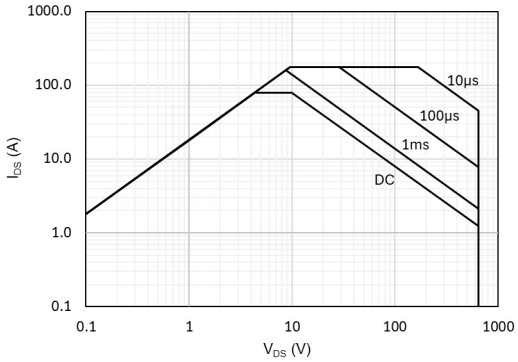
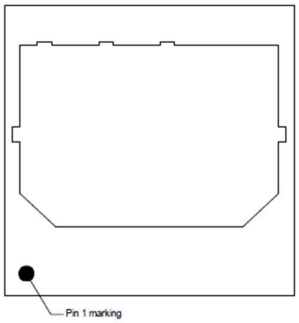


Fig. 15. Safe Operating Area, T_{CASE} = 25°C

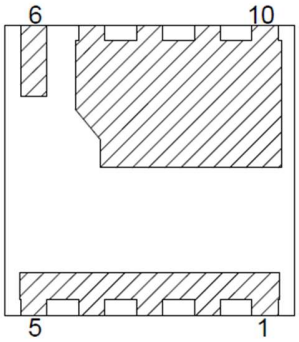
preliminary

10. Pinout Table and P/N Marking

Top



Bottom



PIN		I/O	Description
NUMBER	SYMBOL		
1 – 5	D	P	Drain of GaN FET
6	G	I	Gate of GaN FET
7 - 10	S	O	Source Terminal
BOTTOM PAD	S	O, G	Source of GaN FET and Thermal Pad for Heatsink
TOP PAD	S	O, G	Source of GaN FET and Thermal Pad for Heatsink

Note: I = Input, O = Output, P = Power, G = GaN IC Ground

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11. Drain-to-Source Voltage Considerations

GaN Power FETs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies such as quasi-resonant (QR) or flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 16. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. It is recommended to apply an 80% derating from $V_{DS(TRAN)}$ rating (800V) to 650V max for repetitive V_{DS} spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 16 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (520V) from $V_{DS\ (CONT)}$ (650V). Finally, $V_{DS(TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is < 100 µs.

For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{PLATEAU}$ derating guideline (520V).

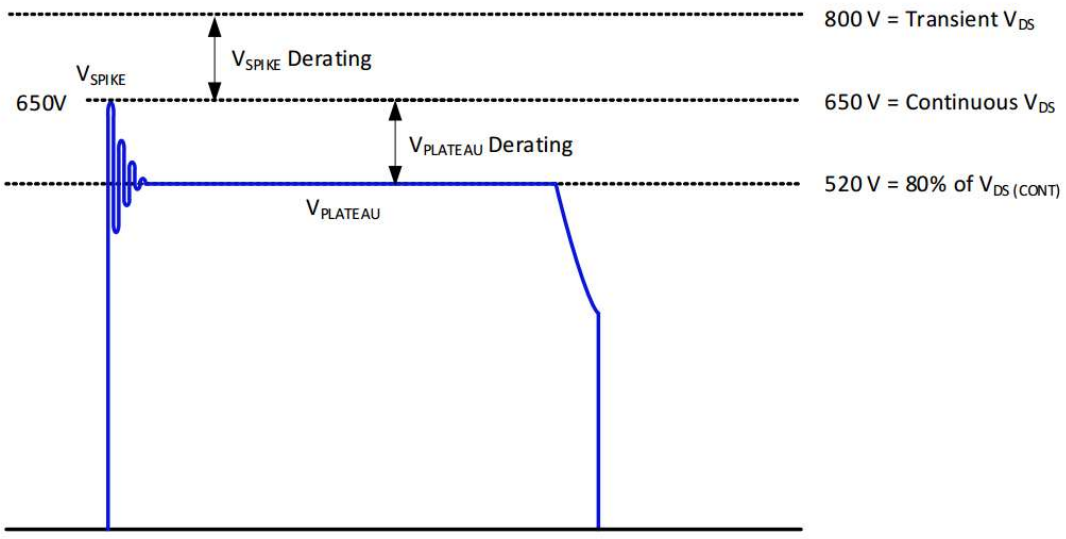


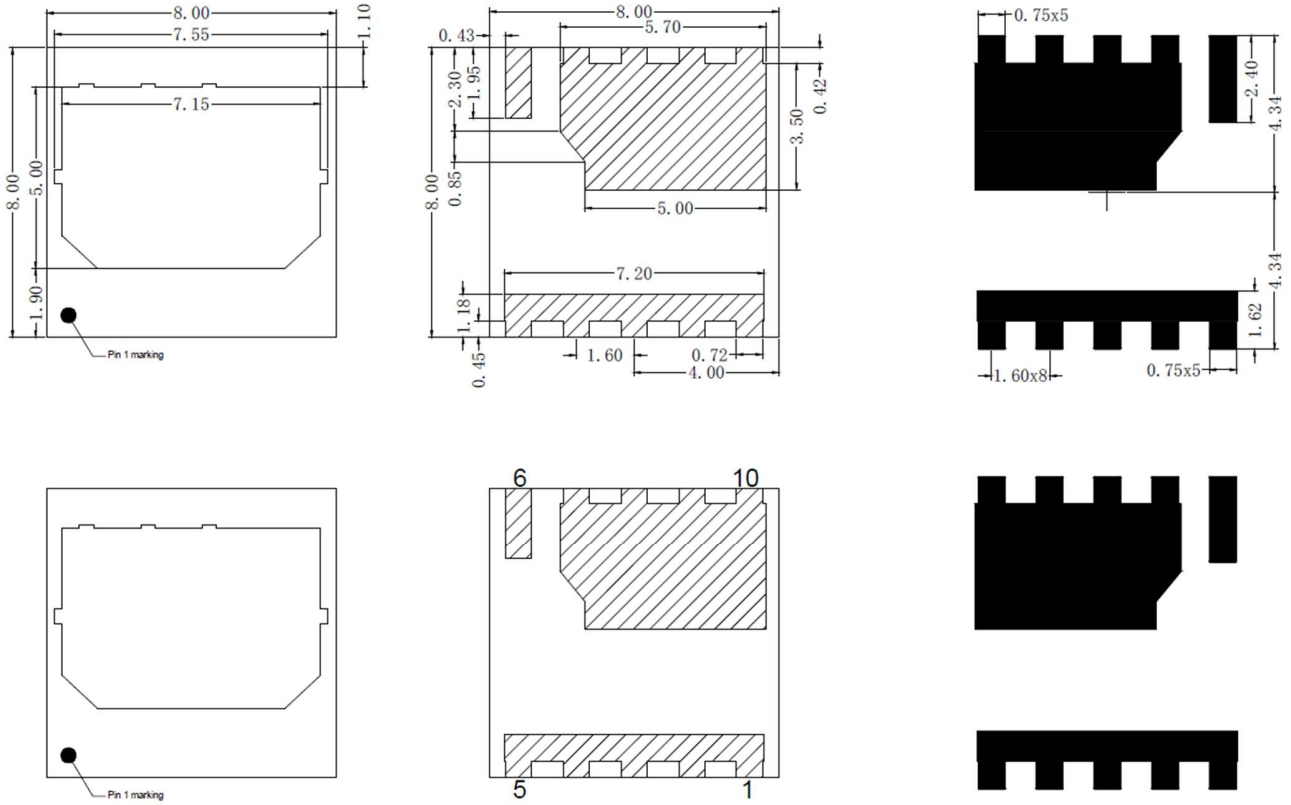
Fig. 16. Typical drain-to-source voltage stress diagram

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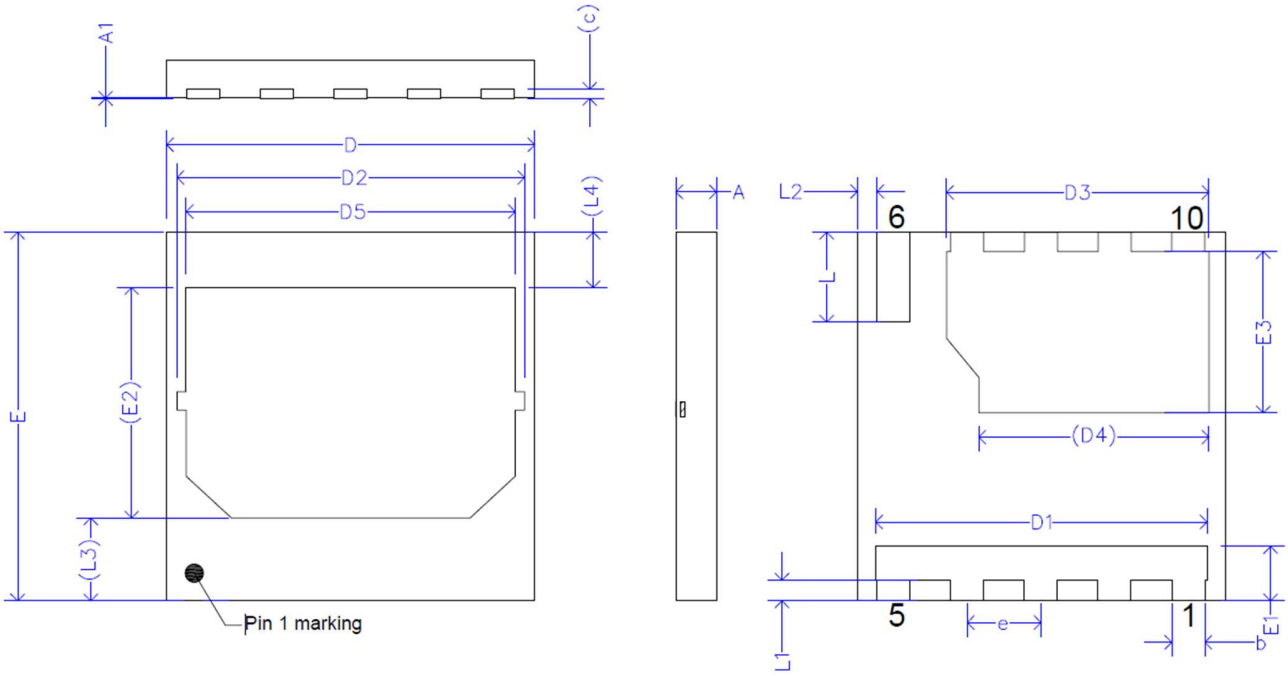
12. PCB Layout Guidelines and PCBA SMT Solder Paste template

PCB layout is critical for thermal management, noise immunity, and proper operation of the device. The following rules should be followed carefully during the design of the PCB layout:

- System-level thermal design for top-cooled packages must observe co-planarity and electrical isolation requirements when multiple power devices are cooled by the same heatsink (Cold Plate). Also, while the majority of heat is transferred through the top-side thermal pad, placing a Cu Plane below the package (shown below) also transfers heat to the board.

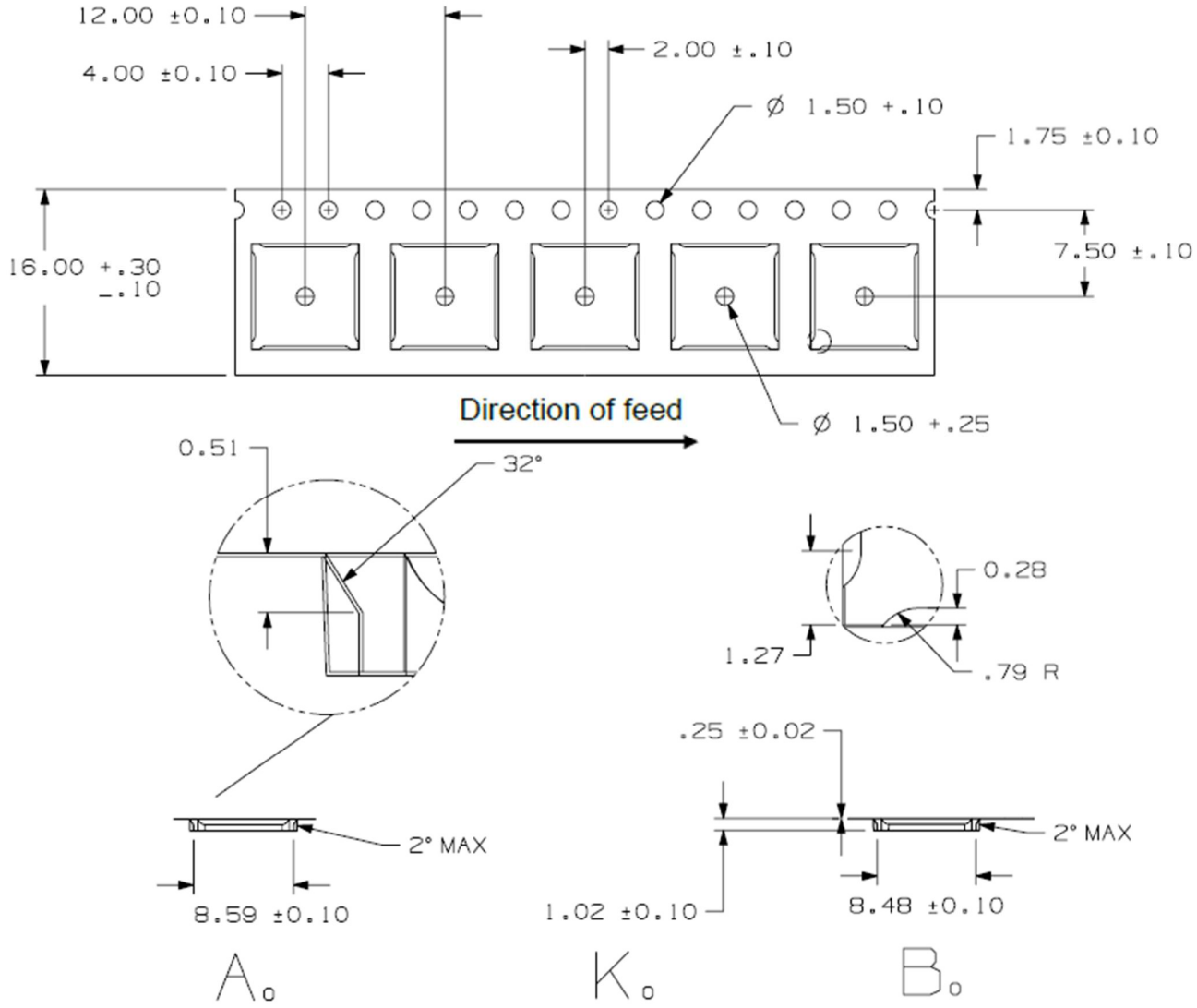


13. Package Outline Dimensions:



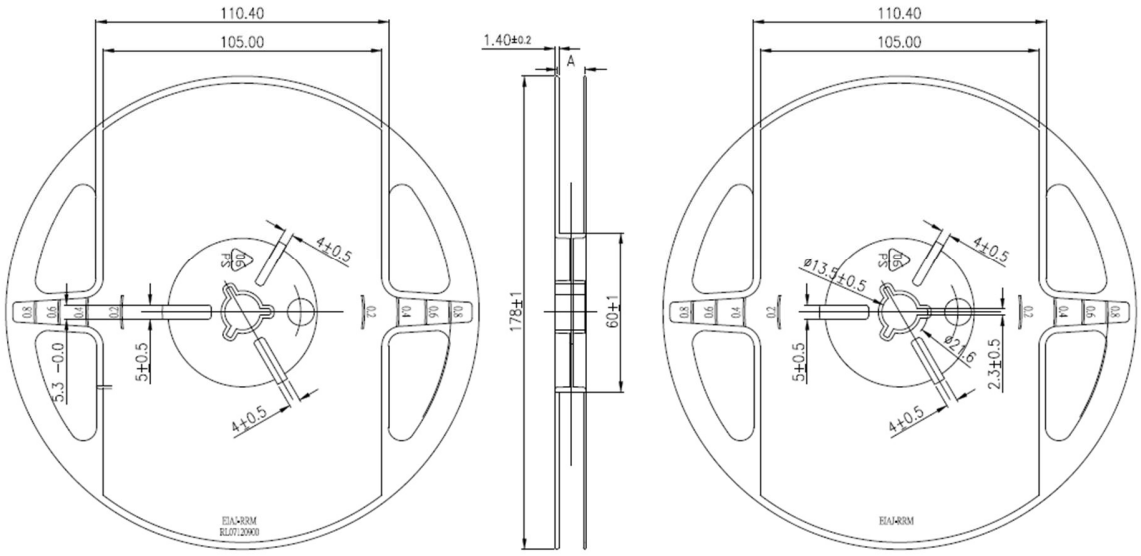
DIM . SYM	MIN	NOM	MAX	Note :
A	---	---	0.95	1. All dimensions are in millimeters 2. Pin 1 identifier is laser marked 3. Pins are finished with NiPdAu plating 4. Dimensions do not include burrs and flashes
A1	---	---	0.01	
b	0.69	0.72	0.75	
c		0.203 REF		
D	---	8.00	---	
D1	7.10	7.20	7.30	
D2	---	7.55	---	
D3	5.60	5.70	5.80	
D4	---	5.00	---	
D5	7.00	7.15	7.30	
E	---	8.00	---	
E1	1.08	1.18	1.28	
E2	---	5.00	---	
E3	---	3.50	---	
e	---	1.60	---	
L	1.85	1.95	2.05	
L1	0.35	0.45	0.55	
L2	0.35	0.45	0.55	
L3	---	1.80	---	
L4	---	1.20	---	

14. TnR Drawing



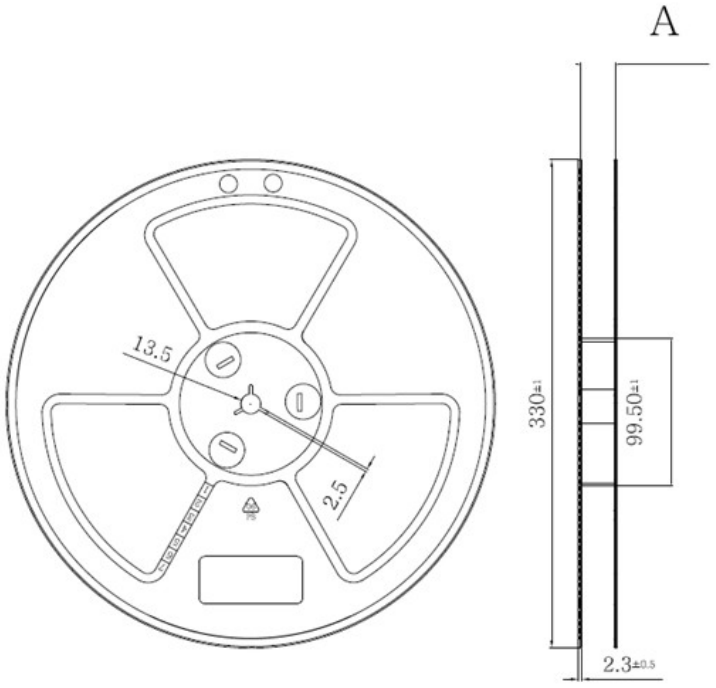
TnR Drawing (Cont.)

7” Reel



A ±1
8.7
12.7
16.7
24.7
32.7

13” Reel



A ±0.5
8.6
12.6
16.6
24.6
32.6
44.6
56.6
72.6

15. Ordering Information

Part Number	Qualification	Package	MSL Rating	TnR Sizes/Qtys
NV6036-RA	JEDEC	DFN 8x8 mm Top-cooled SMD	3	1,000: 7” Reel
NV6036	JEDEC	DFN 8x8 mm Top-cooled SMD	3	4,000: 13” Reel

16. Revision History

Date	Status	Notes
Nov 24th, 2025	Initial Release	• Preliminary Datasheet
Jan 20th, 2026	Preliminary	• Add data and graphs
Jul 06th, 2026	Preliminary	• Update POD and T&R

preliminary

Additional Information

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